GigaDevice Semiconductor Inc.

GD32F10x Hardware Development Guide

Application Note
AN076

Revision 1.3

(Dec. 2024)

Table of Contents

List of Figures

List of Tables

1. Introduction

This article is specially provided for developers of 32-bit general-purpose MCU GD32F10x series based on Arm® Cortex®-M3 architecture. It provides an overall introduction to the hardware development of GD32F10x series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application note is to allow developers to quickly get started and use GD32F10x series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note guide is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32F10x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32F10x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32F10x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32F10x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32F10x series.
6. Reference circuit and PCB Layout design, mainly introduces GD32F10x series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32F10x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32F10x series products.

Table 1-1. Applicable Products

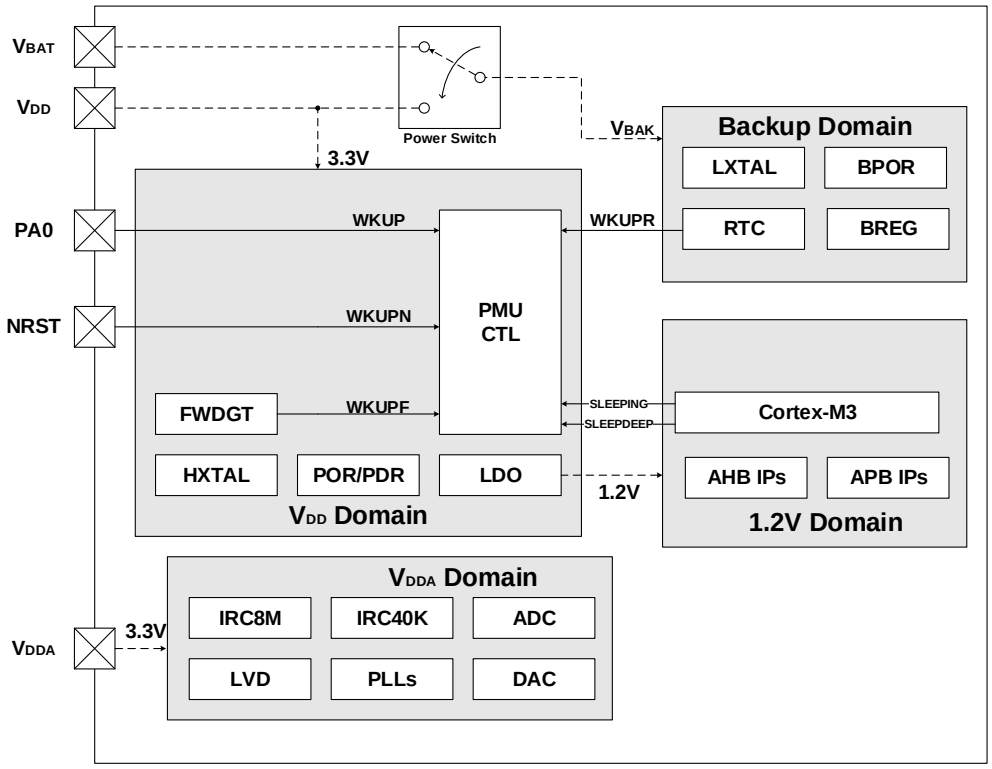
Type	Part Numbers
MCU	GD32F101xx series
	GD32F103xx series
	GD32F105xx series
	GD32F107xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32F10x series products is 2.6V ~ 3.6V.there are three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain, and Backup domain, as is shown in ***Figure 2-1. GD32F10x Series Power supply overview***.The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32F10x Series Power supply overview



LVD:Low Voltage Detector
LDO: Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
PDR: Power Down Reset
BREG: Backup registers

2.1.1. Backup domain

The backup domain supply voltage range is 1.8 V ~ 3.6 V. In order to ensure the content of the Backup domain registers and the RTC supply, when V_{DD} supply is shut down, V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or by another source. But when V_{DD} is connected, even if the V_{BAT} pin is powered by an external battery, etc., V_{BAK} is still powered by V_{DD}.

If no external battery is used in the application, it is recommended to connect V_{BAT} pin externally to V_{DD} pin with a 100nF external ceramic decoupling capacitor.

Note: If the V_{BAT} pin is left floating, the Power Switch will switch V_{BAK} to V_{DD} after the MCU is powered on, and the internal V_{DD} will directly supply power to the Backup domain.

2.1.2. V_{DD} / V_{DDA} Power domain

V_{DD} / V_{DDA} power domain supplies power to all areas except the backup domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two is required to be no more than 300mV (the internal V_{DDA} and V_{DD} are connected by back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. There is a V_{REF} pin (2.4 V ≤ V_{REFP} ≤ V_{DDA}, V_{REFN} = V_{SSA}) for ADC independent power supply on the large package.

- 100 and more pin package chips contain V_{REFP} and V_{REFN}, V_{REFP} can use an external reference power supply, or can be directly connected to V_{DDA}, V_{REFN} must be connected to V_{SSA}.
- 64 and less pin package chips do not have V_{REFP} and V_{REFN}, they are directly connected to V_{DDA} and V_{SSA} internally, and all analog modules are powered by V_{DDA} (including ADC/DAC).

2.1.3. Power supply design

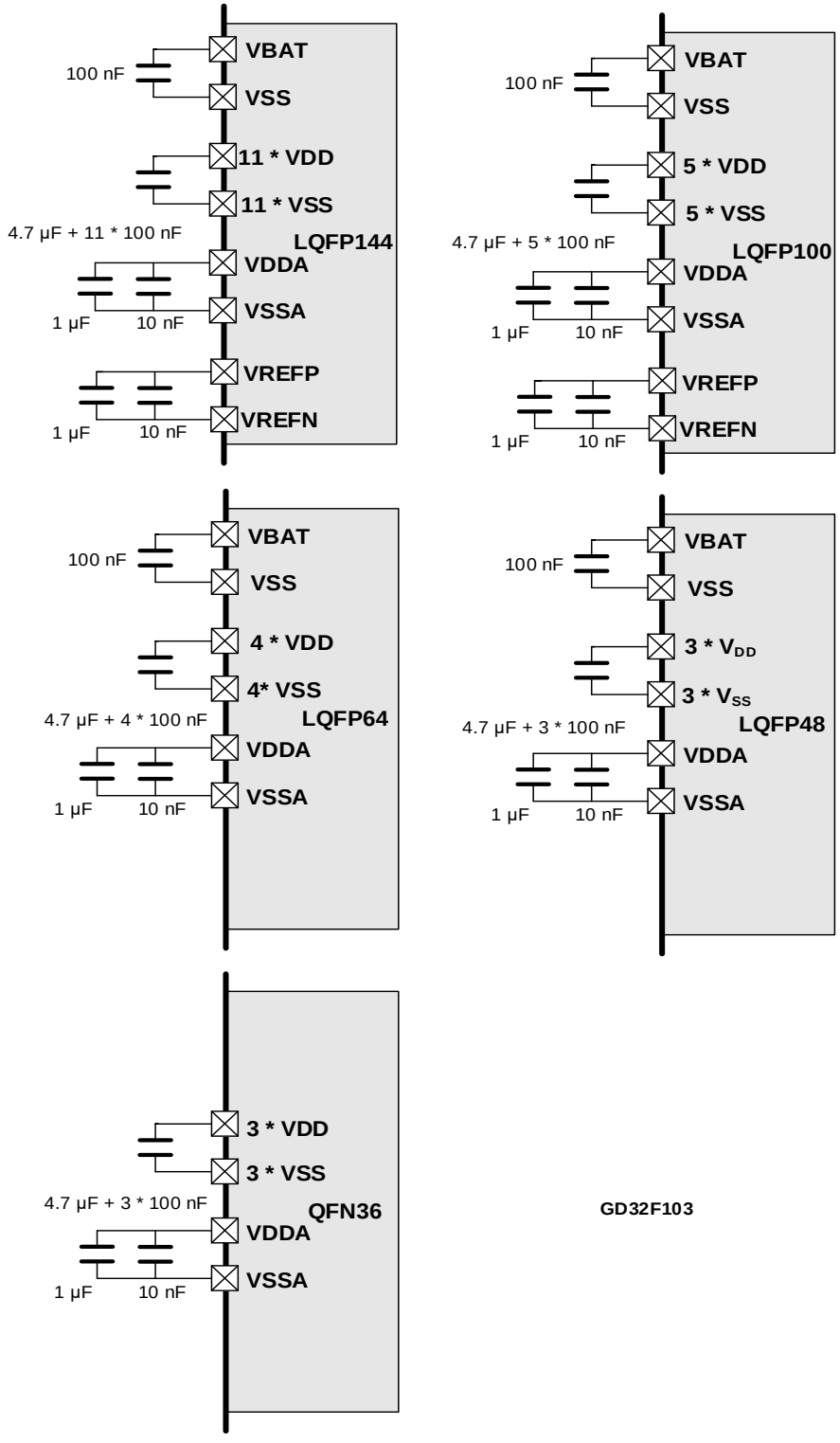
The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- VDD pin must be connected to an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- VDDA pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).
- VBAT pin must be connected to an external battery (1.8 V ~ 3.6 V). If there is no external battery, it is recommended to connect the VBAT pin to the ground through a 100nF capacitor and then connect it to the VDD pin.
- VREFP pin can be directly connected to VDDA. If a separate external reference voltage is used on VREF (1.8V ≤ VREFP ≤ VDDA, VREFN = VSSA), a 10nF+1uF ceramic capacitor must also be connected to ground on the VREFP pin.
- Even though all VDD's are connected internally and all VSS are connected internally, all VDD's must be connected together and all VSS must be connected together outside the chip.
- VDDA partially supplies power to all analog circuits, including ADC module, reset

circuit, PVD(programmable voltage Monitor), PLL, power-on reset (POR) and power-off reset (PDR) modules, switches that control VBAT switching, etc.

- Even if you do not use ADC function, you need to connect to VDDA.
- It is strongly recommended that VDD and VDDA use the same power supply.
- The voltage difference between the VDD and VDDA cannot exceed 300mV. The VDD and VDDA should be powered on or off at the same time.

Figure 2-2. GD32F10x Recommend Power Supply Design



Note:

1. All decoupling capacitors need to be as close as possible to the pins on the PCB board.
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
3. LQFP64，LQFP48，QFN36: VREFP and VDDA are connected internally, VREFN and VSSA are connected internally.

2.2. Medium density, high density and ultra-high density power supply detection, reset and timely clock

The GD32F101xx and GD32F103xx flash memory capacities between 16K and 128K bytes are called medium density products (GD32F10x_MD).

The flash memory capacity of GD32F101xx and GD32F103xx is between 256K and 512K bytes, which is called high-density product (GD32F10x_HD).

Products with flash memory capacity greater than 512K bytes on GD32F101xx and GD32F103xx are called ultra-high density products (GD32F10x_XD).

This section is based on the GD32F10x series chip of version A, and the default VDD and VDDA pins remain connected and are powered by the same power supply.

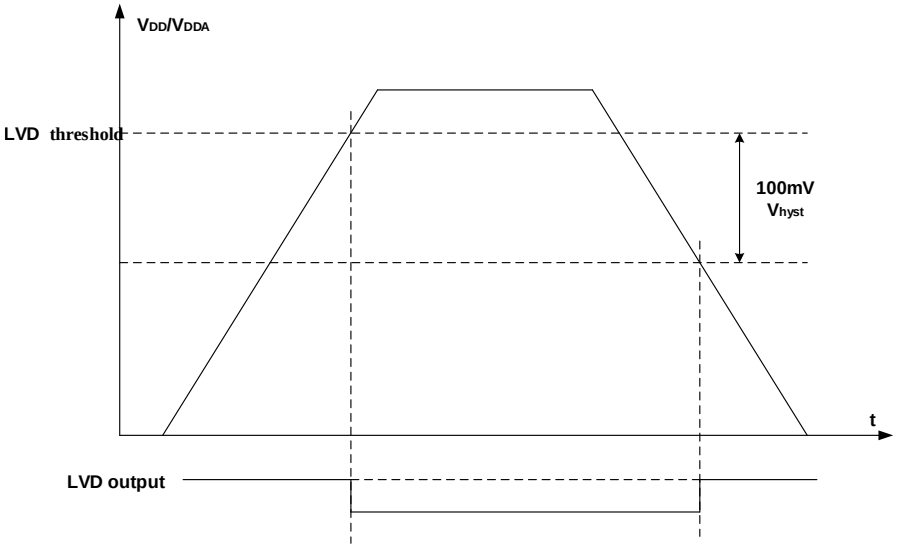
GD32F10x series reset control includes three types of reset: power reset, system reset and backup domain reset.The power reset is cold reset. When the power is started, all systems except the backup domain are reset.In the process of power and system reset, NRST will maintain a low level until the end of reset.When MCU cannot be executed, the oscilloscope can monitor the NRST pin waveform to determine whether the chip has been reset events.

2.2.1. LVD

The function of LVD is to detect whether the V_{DD} / V_{DDA} supply voltage is below the low voltage detection threshold (2.2V ~ 2.9V), which is configured by the LVDT[2:0] bit in the power control Register (PMU_CTL).LVD is enabled by LVDEN setting. The LVDF bit in the Power Status Register (PMU_CS) indicates the occurrence of a low-voltage event, which is connected to line 16 of EXTI. The user can generate the corresponding interrupt by configuring line 16 of EXTI.The LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16.The hysteresis voltage Vhyst value is 100mV.

LVD application: when MCU power is affected by external interference, such as voltage sag, we can set the low voltage detection threshold through LVD (it is recommended to set the threshold greater than PDR value), once the fall to the threshold, LVD interrupt is opened, can be set in the interrupt function soft reset and other operations, to avoid other MCU anomalies.

Figure 2-3. LVD Threshold Waveform



2.2.2. POR / PDR

The POR/PDR (Power on/power off reset) circuit is integrated inside the chip to detect the V_{DD}/V_{DDA} and generate a power reset signal when the voltage is below a specific threshold to reset the entire chip except the backup domain.For GD32F101xx and GD32F103xx whose flash capacity is less than 128KB, V_{POR} indicates the threshold voltage for power-on reset, and the typical value is about 2.4V. V_{PDR} indicates the threshold voltage for power-off reset, and the typical value is about 2.35V. The hysteretic voltage Vhyst is about 50mV.For the GD32F103xx product whose flash capacity is larger than 128KB, V_{POR} indicates the threshold voltage for power-on reset (the typical value is about 2.4V), V_{PDR} indicates the threshold voltage for power-off reset (the typical value is about 1.8V), and hysteretic voltage Vhyst is about 600mV.

Figure 2-4. Power-on/power-off and resetting waveform of GD32F101xx and GD32F103xx whose flash capacity does not exceed 128KB

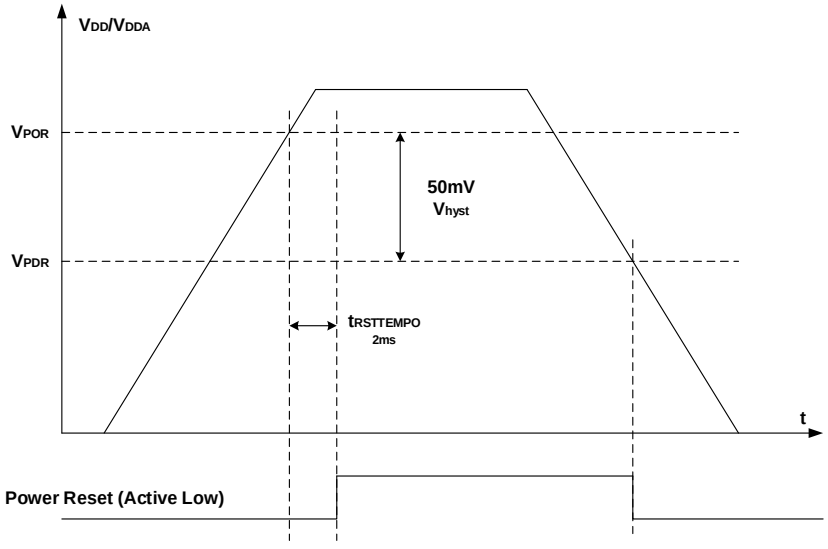
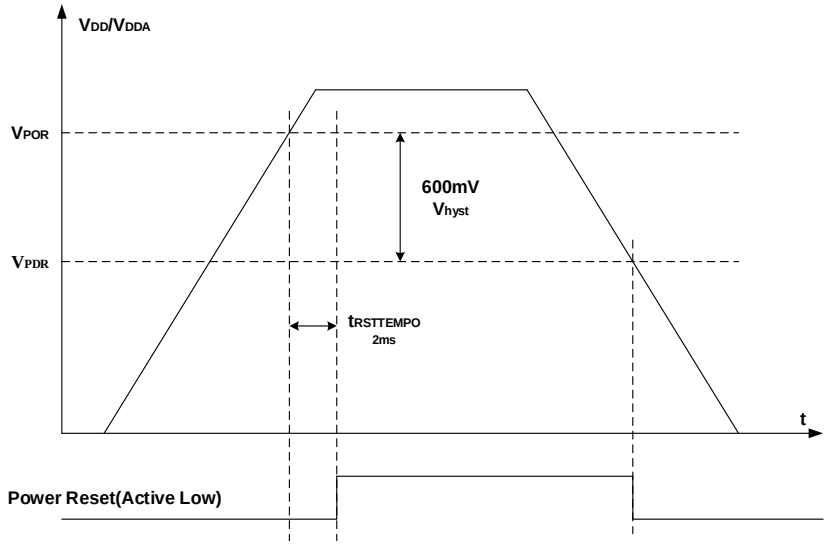


Figure 2-5. Power-on/power-off resetting waveform of a GD32F103xx product larger than 128KB



2.2.3. NRST Pin

In addition, MCU reset source can be determined by the query of register RCU_RSTSCK (0x40021024), the register can only be reset on power to clear the flag bit, so in the process of use, after the reset source is obtained, the reset flag can be cleared by RSTFC control bit, so that when watchdog reset or other reset events occur,To be more accurate in the RCU_RSTSCK register is reflected:

Figure 2-6. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPRSTF	WWDGTRSTF	FWDGTRSTF	SWRSTF	PORRSTF	EPRSTF	Reserved	RSTFC	Reserved							
r	r	r	r	r	r		rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														IRC40KSTB	IRC40KEN
														r	rw

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs. To prevent a false trigger reset, the NRST pin is recommended to place a capacitor (typically 100nF).

Figure 2-7. System Reset Circuit

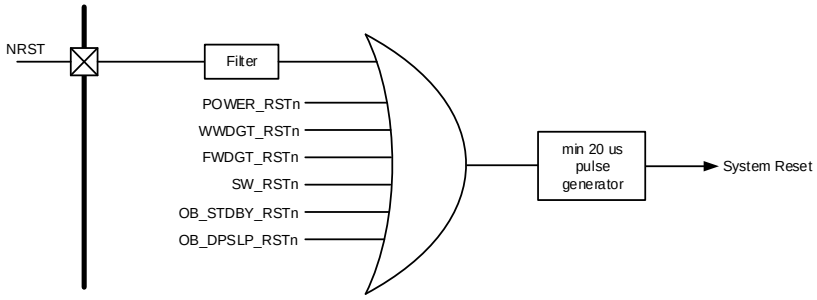
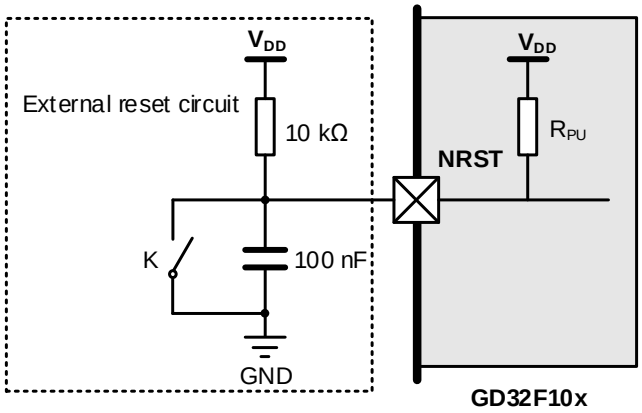


Figure 2-8. Recommend External Reset Circuit

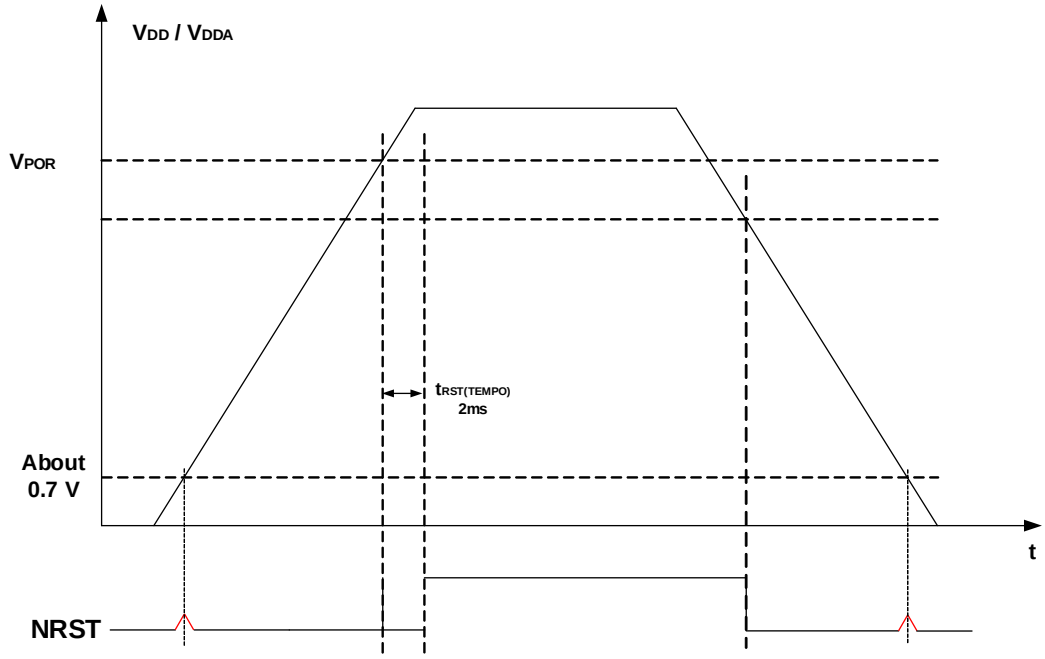


Note:

1. The internal pull-up resistor R_{PU} is 40 kΩ. the pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS tube, when VDD/VDDA < 0.7V during the chip power-on and power-off process, pulling down the MOS tube inside the chip will not pull down the NRST pin. That is, when VDD/VDDA ≈ 0.7V is used during the chip power-on and power-off process, a tiny pulse will occur, which does not affect the normal operation of the chip, as shown in ***Figure 2-9. NRST pin power-on and power-off MOS tube pulse diagram***.

Figure 2-9. NRST pin power-on and power-off MOS tube pulse diagram



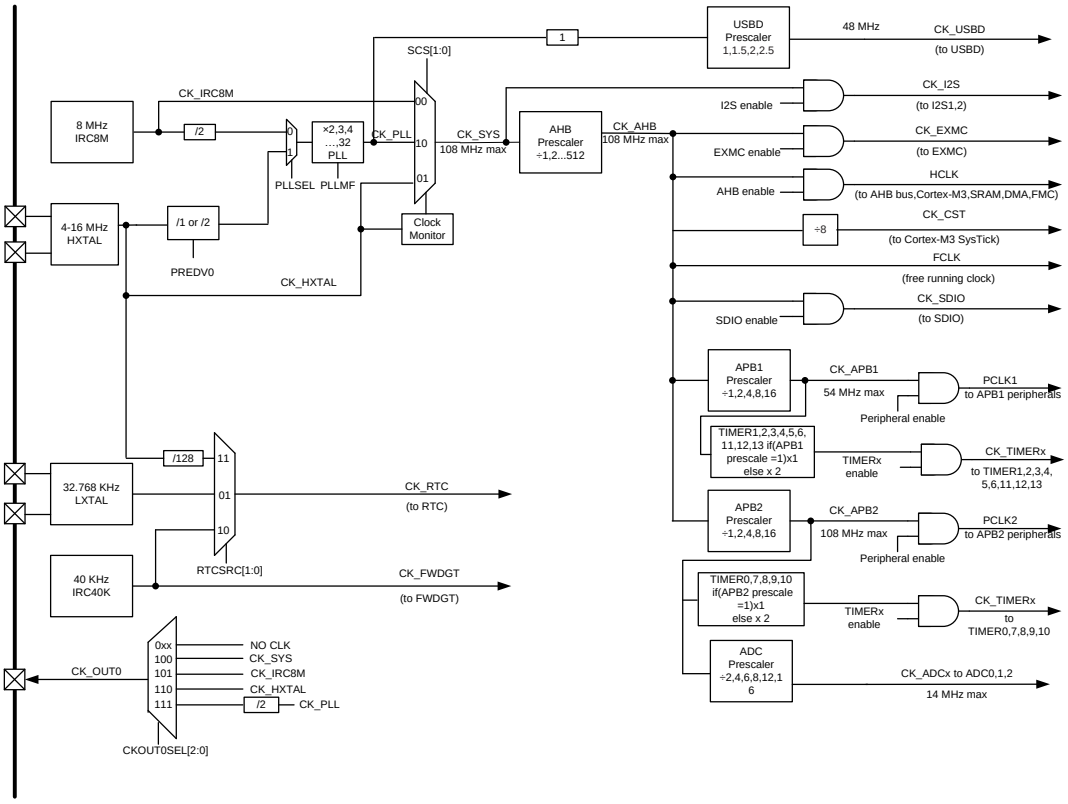
Due to the difference in charging and discharging speed, the pulse duration of the falling edge is longer than that of the rising edge, and the duration of both is ms class.

2.2.4. Clock

GD32F101xx / GD32F103xx series has a complete clock system inside. You can choose the appropriate clock source according to different applications. The main features of the clock are:

- 4-16 MHz external high-speed crystal oscillator (HXTAL)
- 8 MHz internal high-speed RC oscillator (IRC8M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- 40 kHz internal low speed RC oscillator (IRC40K)
- PLL clock source can be selected from HXTAL or IRC8M
- HXTAL clock can be monitored

Figure 2-10. Clock Tree



2.2.5. External high-speed crystal oscillator clock (HXTAL)

4-16MHz external high-speed crystal oscillator (passive crystal) can provide accurate master clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-11. HXTAL External Crystal Circuit

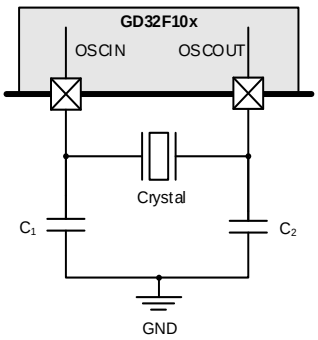
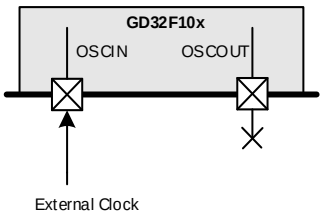


Figure 2-12. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close as possible to the crystal pin.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and causes the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal > external passive crystal > internal IRC8M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.

2.2.6. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low speed external crystal (passive crystal), which can provide a low power and high precision clock source for RTC.The RTC module of MCU is equivalent to a counter, whose accuracy will be affected by crystal performance, matching capacitance and PCB material, etc. In order to obtain better accuracy, it is recommended to connect PC13 to the TIMER input capture pin during circuit design, calibrate LXTAL through TIMER, and set the frequency division register of RTC according to the calibration.LXTAL can also support bypass clock inputs (active crystal, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-13. LXTAL External Crystal Circuit

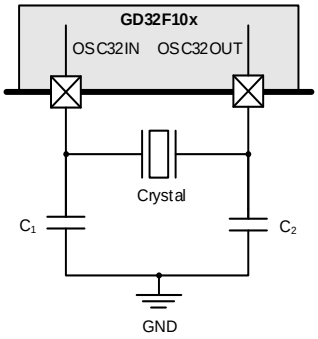
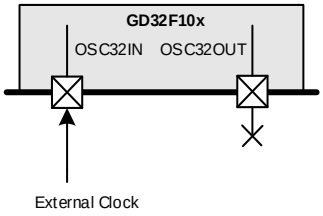


Figure 2-14. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC40K as the clock source and uses the VBAT external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After the power is re-energized, the RTC will continue to accumulate the counting value according to the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.2.7. Clock output capability (CKOUT)

For GD32F10x series MCU, you can select different clock signal output by configuring the CKOUT0SEL[2:0] bits of the clock register RCU_CFG0, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal.

Table 2-1. CKOUT0SEL[2:0] Control Bits

CKOUT0SEL[2:0]	Clock Source
0xx	NA
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL/2

2.2.8. HXTAL Clock monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the clock control register RCU_CTL, HXTAL can enable the clock monitoring function. This function must be enabled after HXTAL start-up delay and disabled after HXTAL is stopped. Once an HXTAL failure is detected, the HXTAL will be automatically disabled, The HXTAL clock blocking interrupt flag bit CKMIF in interrupt register RCU_INT will be set to '1', generating an HXTAL failure event, and the HXTAL fault event is generated. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Cortex®-M3.

Note: If HXTAL is selected as the system clock, PLL or RTC clock source, HXTAL failure will prompt the selection of IRC8M as the system clock source, the PLL will be automatically disabled, and the RTC clock source needs to be reconfigured.

2.3. Power detection, reset and timely clock of connected products

GD32F105xx and GD32F107xx microcontrollers are called interconnected products (GD32F10x_CL).

This section is based on the GD32F10x series chip of version A, and the default VDD and VDDA pins remain connected and are powered by the same power supply.

GD32F10x series reset control includes three types of reset: power reset, system reset and backup domain reset.The power reset is cold reset. When the power is started, all systems except the backup domain are reset.In the process of power and system reset, NRST will maintain a low level until the end of reset.When MCU cannot be executed, the oscilloscope can monitor the NRST pin waveform to determine whether the chip has been reset events.

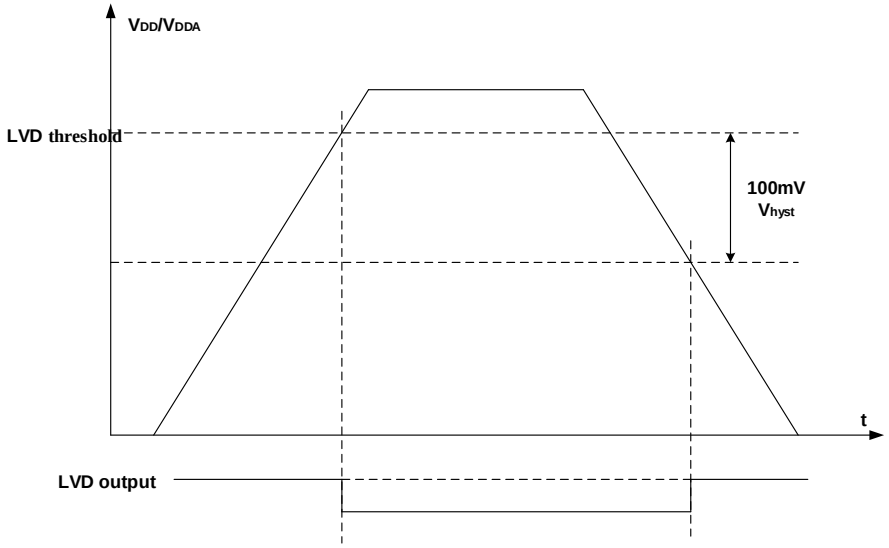
2.3.1. LVD

The function of LVD is to detect whether the V_{DD} / V_{DDA} supply voltage is below the low voltage detection threshold (2.2V ~ 2.9V), which is configured by the LVDT[2:0] bit in the power control Register (PMU_CTL).LVD is enabled by LVDEN setting. The LVDF bit in the Power Status Register (PMU_CS) indicates the occurrence of a low-voltage event, which is connected to line 16 of EXTI. The user can generate the corresponding interrupt by configuring line 16 of

EXTI.The LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16.The hysteresis voltage Vhyst value is 100mV.

LVD application: when MCU power is external interference, such as the occurrence of voltage sag, we can set the low voltage detection threshold through LVD (the threshold is greater than PDR value), once the fall to the threshold, LVD interrupt is opened, can be set in the interrupt function soft reset and other operations, to avoid other MCU anomalies.

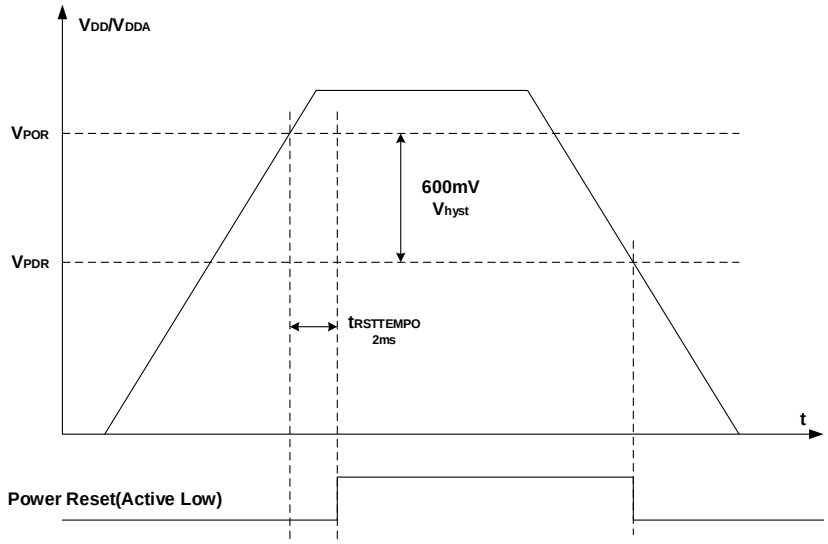
Figure 2-15. LVD Threshold Waveform



2.3.2. POR / PDR

The POR/PDR (Power on/power off reset) circuit is integrated inside the chip to detect the V_{DD}/V_{DDA} and generate a power reset signal when the voltage is below a specific threshold to reset the entire chip except the backup domain.V_{POR} indicates the threshold voltage for power-on reset, which is about 2.4 V. V_{PDR} indicates the threshold voltage for power-off reset, which is about 1.8V.The hysteresis voltage Vhyst value is about 600mV.

Figure 2-16. Power-on/Power-down Reset Waveforms



Note: Applicable to GD32F105xx, GD32F107xx series products.

2.3.3. NRST Pin

In addition, MCU reset source can be determined by the query of register RCU_RSTSCK (0x40021024), the register can only be reset on power to clear the flag bit, so in the process of use, after the reset source is obtained, the reset flag can be cleared by RSTFC control bit, so that when watchdog reset or other reset events occur,To be more accurate in the RCU_RSTSCK register is reflected:

Figure 2-17. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPRSTF	WWDGTRSTF	FWDGTRSTF	SWRSTF	PORRSTF	EPRSTF	Reserved	RSTFC	Reserved							
r	r	r	r	r	r		rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														IRC40KSTB	IRC40KEN

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs. To prevent a false trigger reset, the NRST pin is recommended to place a capacitor (typically 100nF).

Figure 2-18. System Reset Circuit

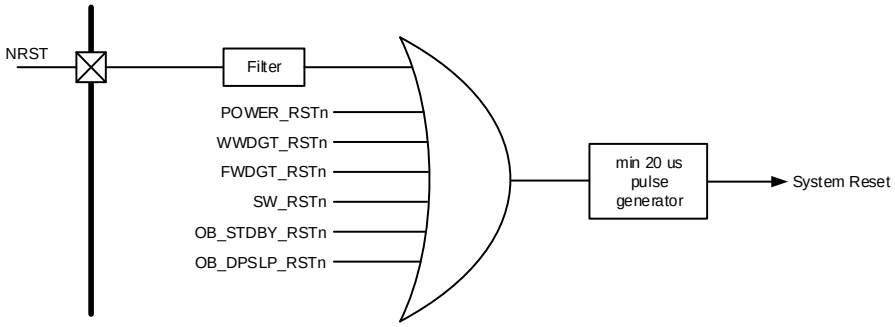
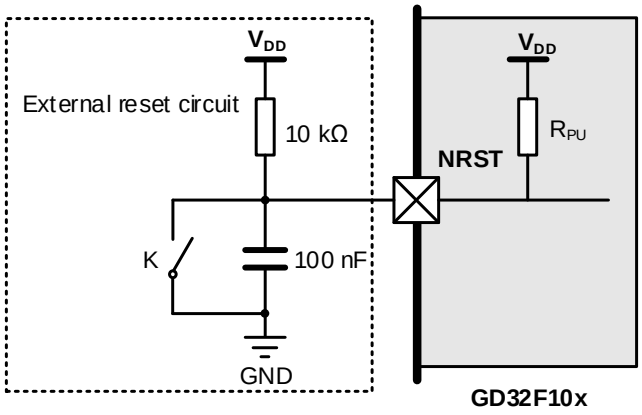


Figure 2-19. Recommend External Reset Circuit

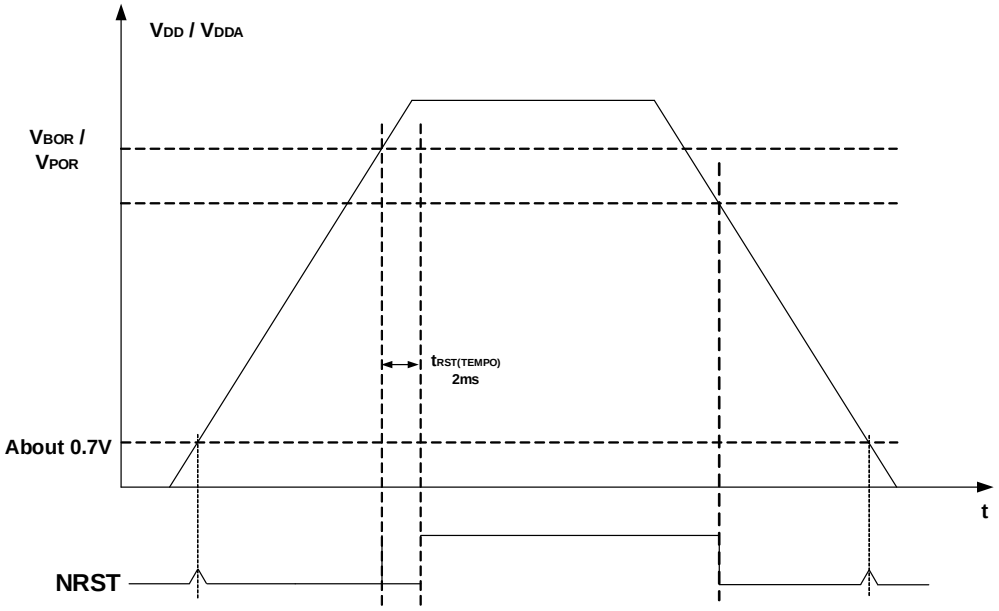


Note:

1. The internal pull-up resistor R_{PU} is 40 kΩ. You are advised to connect to an external pull-up resistor of 10 kω to ensure that voltage interference does not cause abnormal chip operation
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS tube, when VDD/VDDA < 0.7V during the chip power-on and power-off process, pulling down the MOS tube inside the chip will not pull down the NRST pin. That is, when VDD/VDDA ≈ 0.7V is used during the chip power-on and power-off process, a tiny pulse will occur, which does not affect the normal operation of the chip, as shown in ***Figure 2-20. NRST pin power-on and power-off MOS tube pulse diagram***.

Figure 2-20. NRST pin power-on and power-off MOS tube pulse diagram



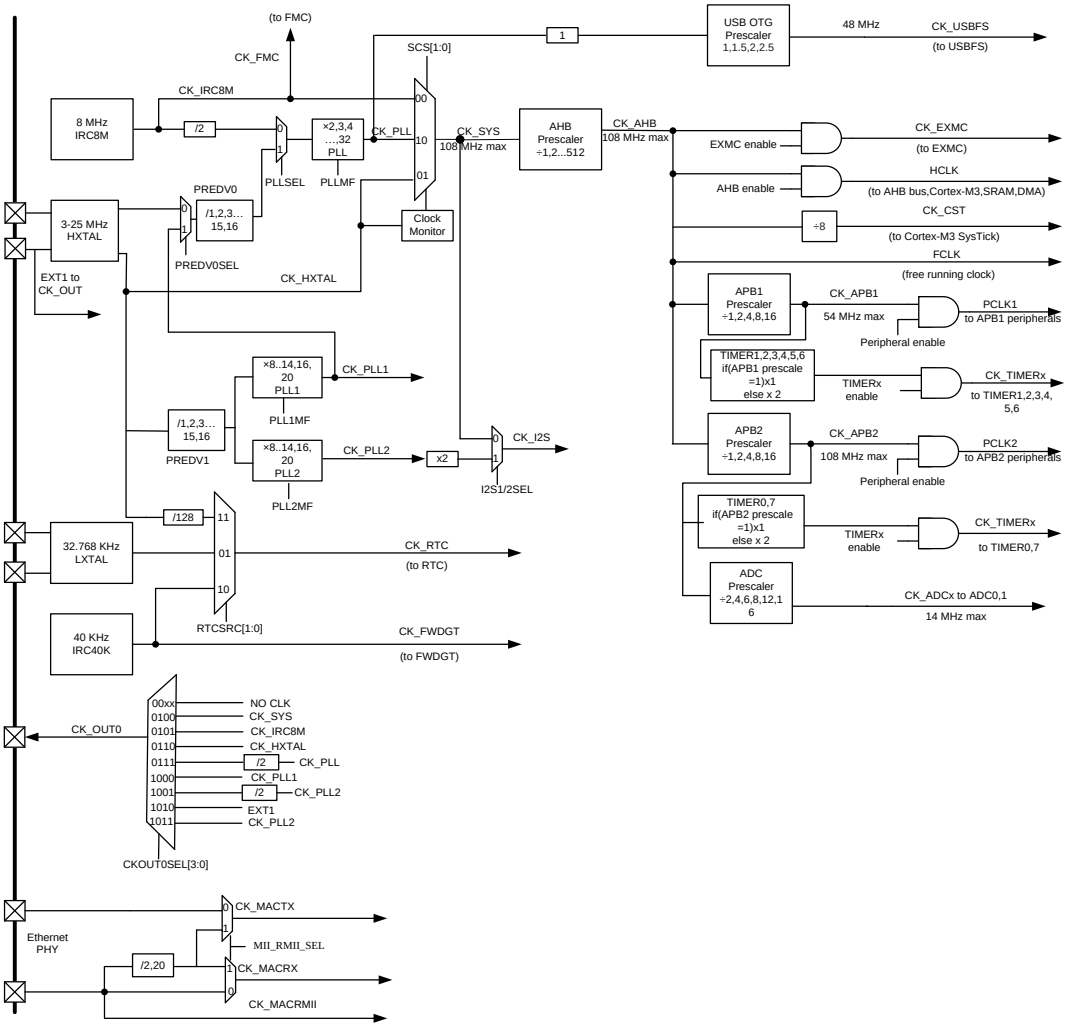
Due to the difference in charging and discharging speed, the pulse duration of the falling edge is longer than that of the rising edge, and the duration of both is ms class.

2.3.4. Clock

GD32F105xx and GD32F107xx series have a complete internal clock system, you can choose the appropriate clock source according to different application occasions, the main features of the clock:

- 3-25 MHz external high-speed crystal oscillator (HXTAL)
- 8 MHz internal high-speed RC oscillator (IRC8M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- 40 kHz internal low speed RC oscillator (IRC40K)
- PLL clock source can be selected from HXTAL, IRC8M or IRC48M
- HXTAL clock can be monitored

Figure 2-21. Clock Tree



2.3.5. External high-speed crystal oscillator clock (HXTAL)

3-25MHz external high-speed crystal oscillator (passive crystal) can provide accurate master clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-22. HXTAL External Crystal Circuit

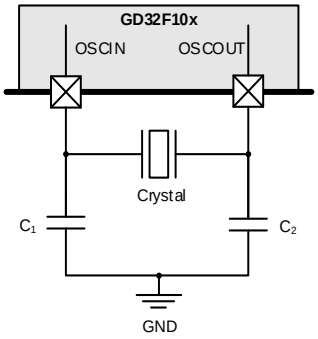
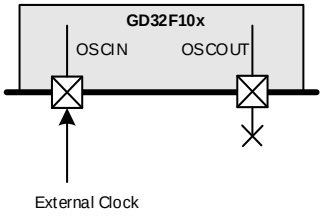


Figure 2-23. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close as possible to the crystal pin.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and causes the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal > external passive crystal > internal IRC8M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}. If Bypass is not turned on, the amplitude requirements of the active crystal oscillator will be greatly reduced.

2.3.6. External low-speed crystal oscillator clock（LXTAL）

The LXTAL is an external low speed crystal or ceramic resonator with a frequency of 32.768kHz. It provides a low power consumption and high precision clock source for real-time

clock circuit. The LXTAL oscillator can be started and turned off by setting the LXTALEN bit in the backup domain control register (RCU_BDCTL). The LXTALSTB bit in the backup domain control register RCU_BDCTL is used to indicate whether the LXTAL clock is stable. If the corresponding interrupt enable bit LXTALSTBIE in the interrupt register RCU_INT is set to '1', an interrupt will be generated after LXTAL stabilizes.

The LXTALBPS and LXTALEN positions' 1 'of the domain control register RCU_BDCTL can be backed up to select external clock bypass mode. CK_LXTAL is consistent with the external clock signal connected to OSC32IN pins.

Figure 2-24. LXTAL External Crystal Circuit

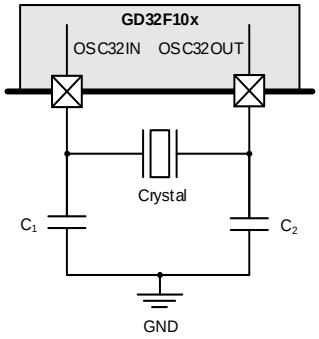
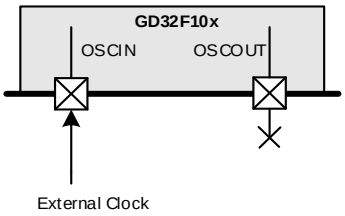


Figure 2-25. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC40K as the clock source and uses the VBAT external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After the power is re-energized, the RTC will continue to accumulate the counting value according to the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.3.7. Clock output capability (CKOUT)

For GD32F10x series MCU, you can select different clock signal output by configuring the CKOUT0SEL[3:0] bits of the clock register RCU_CFG0, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal.

Table 2-2. CKOUT0SEL[3:0] Control Bits

CKOUT0SEL[3:0]	Clock Source
00xx	NO CLK
0100	CK_SYS
0101	CK_IRC8M
0110	CK_HXTAL
0111	CK_PLL/2
1000	CK_PLL1
1001	CK_PLL2/2
1010	EXT1
1011	CK_PLL2

2.3.8. HXTAL Clock monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the clock control register RCU_CTL, HXTAL can enable the clock monitoring function. This function must be enabled after HXTAL start-up delay and disabled after HXTAL is stopped. Once an HXTAL failure is detected, the HXTAL will be automatically disabled, The HXTAL clock blocking interrupt flag bit CKMIF in interrupt register RCU_INT will be set to '1', generating an HXTAL failure event, and the HXTAL fault event is generated. The interrupt caused by this fault is connected to the non-maskable interrupt NMI.

Note: If HXTAL is selected as the system clock, PLL or RTC clock source, HXTAL failure will prompt the selection of IRC8M as the system clock source, the PLL will be automatically disabled, and the RTC clock source needs to be reconfigured.

2.4. Startup Configuration

GD32F10x series provides three boot modes, which can be selected by the BOOT0 bit and the BOOT1 pin to determine the boot option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND; when running the System Memory to update the program, you need to connect the BOOT0 pin to high and the BOOT1 pin to low. After the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

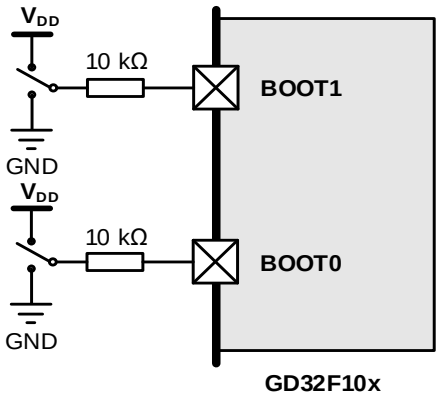
The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In GD32F10x devices, the Bootloader can interact with the outside world

through USART0 (PA9 and PA10).

Table 2-3. Bootloader Mode

BOOT Mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-26. Recommend BOOT Circuit Design



Note:

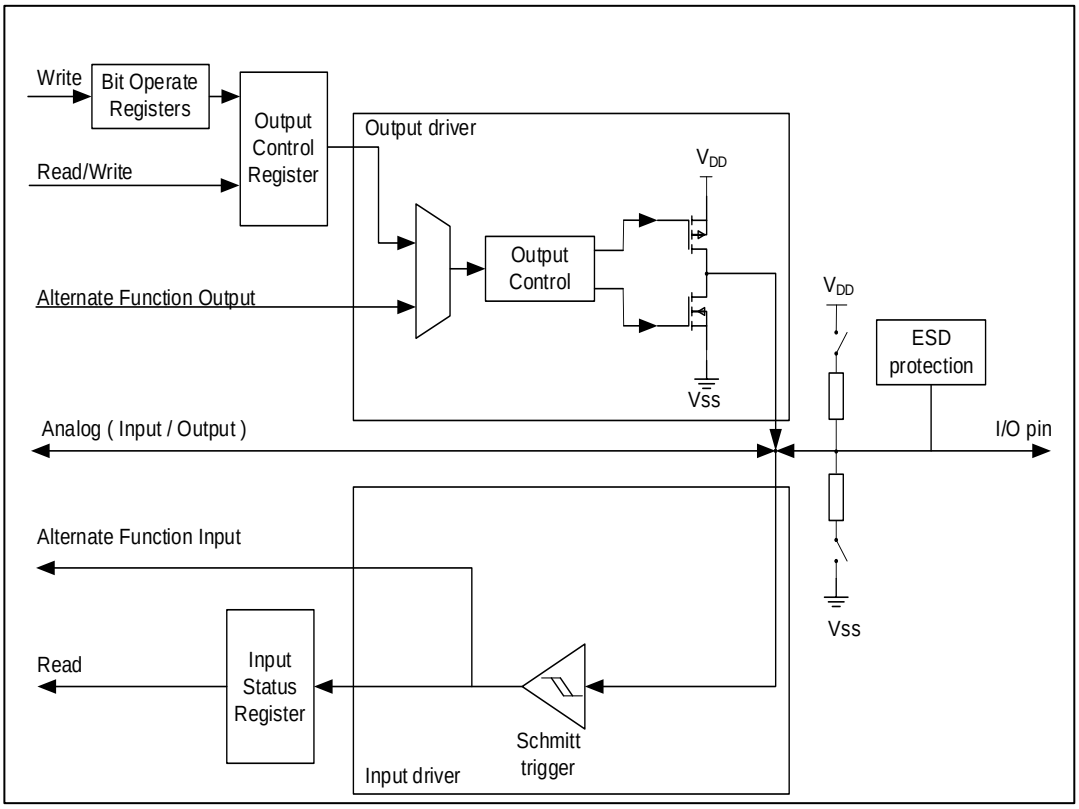
1. After the MCU is running, if the BOOT status is changed, it will take effect after the system is reset.
2. Once the BOOT1 pin state is sampled, it can be released for other purposes.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

The GPIO interface includes 5 groups of general-purpose input/output ports, each group of ports provides up to 16 general-purpose input/output pins, which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15 and PE0 ~ PE15, each pin can be independently configured through registers, the basic structure of GPIO port is shown in the following figure.

Figure 2-27. Basic Structure of Standard IO



Note:

1. The IO port is divided into 5V tolerance and non-5V tolerance. When using, pay attention to distinguish the voltage tolerance of the IO port, see Datasheet for details.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. Non-5v tolerance IO, external voltage exceeding VDD, may produce irrigation current.
4. GD32F103xx 5V tolerance pin, pull up input can not pull 3.3V, can only pull up to 2.6V.
5. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
6. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
7. The drive capability of the three IO ports PC13, PC14, and PC15 is weak, and the output current capability is limited (about 3mA). When configured in output mode, the operating speed cannot exceed 2MHz (the maximum load is 30pF).
8. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
9. IO driving LED, it is recommended to consider the use of irrigation current as far as possible.

2.5.2. USART Circuit

Universal Synchronous Asynchronous Receiver Transmitter (USART) provides a flexible and convenient serial data exchange interface, and data frames can be transmitted in full-duplex or half-duplex, synchronous or asynchronous mode. The USART provides a programmable baud rate generator that divides the system clock to generate the specific frequency required for USART transmission and reception.

USART not only supports the standard asynchronous transceiver mode, but also implements some other types of serial data exchange modes, such as infrared coding specification, SIR, smart card protocol, LIN, and synchronous single-duplex mode. It also supports multiprocessor communication and Modem flow control operation (CTS/RTS). Data frames support transmission from the LSB or MSB. Both the polarity of the data bits and the TX/RX pins can be flexibly configured.

USART supports DMA function to realize high-speed data communication.

Table 2-4. USART Important Pin Description

Pin	Type	Description
RX	Input	Receive data
TX	Output I/O (Single-Wire Mode/Smart Card Mode)	Send data, when USART is enabled, if no data is sent, the default is high level.
CK	Output	Serial clock signal for synchronous communication
nCTS	Input	Hardware flow control mode send enable signal
nRTS	Output	Hardware flow control mode send request signal

2.5.3. ADC Circuit

The GD32F10x series integrates a 12-bit SAR ADC, which has up to 18 channels and can measure 16 external and 2 internal signal sources. The internal signal is the temperature sensor channel (ADC0_CH16) and the internal reference voltage input channel (ADC0_CH17). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC and is internally connected to ADC0_IN17. The supply voltage of the ADC is 2.4V to 3.6V, and the general supply voltage is 3.3V. ADC input range: $V_{REFN} \leq VIN \leq V_{REFP}$.

Table 2-5. ADC Internal signal

Internal signal name	Signal types	Instructions
V_{SENSE}	Input	Internal temperature sensor voltage output
V_{REFINT}	Input	Internal reference voltage output

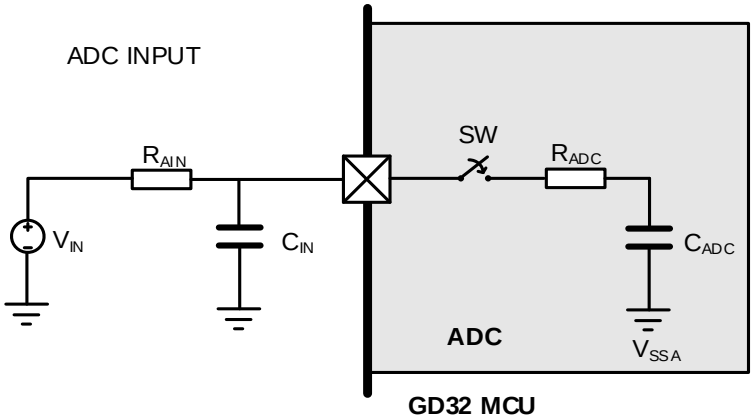
Table 2-6. ADC Pin definition

Name	Signal types	Annotation
V_{DDA}	Input, analog power supply	Analog power input is equal to V_{DD}, 2.6V ≤ V_{DDA} ≤ 3.6V
V_{SSA}	Input, analog power supply ground	Analog, is equal to V_{SS}
V_{REFP}	Input, simulating reference voltage	ADC positive reference voltage, 2.4V ≤V_{REFP} ≤V_{DDA}
V_{REFN}	Input, negative analog reference voltage	ADC negative reference voltage, V_{REFN} = V_{SSA}
ADCx_IN[15:0]	Input, analog signal	Up to 16 external access ways

If the ADC collects the external input voltage in the process of use, if the sampled data fluctuates greatly, it may be due to the interference caused by the fluctuation of the power supply. It can be calibrated through the sampling internal V_{REFINT} to invert the external sampling voltage.

When designing ADC circuit, it is recommended to place a small capacitor at the ADC input pin, and a small capacitor of 500pF is recommended.

Figure 2-28. ADC Acquisition Circuit Design



When f_{ADC} = 42MHz, the relationship between input impedance and sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible, and select a larger sampling period as much as possible. In the design of external circuit, input impedance should also be reduced as much as possible.

Table 2-7. f_{ADC}=42MHz Relationship between Sampling period and External input impedance

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
1.5	0.11	0.1
7.5	0.54	1.5
13.5	0.96	2.9
28.5	2.04	6.3
41.5	2.96	9.3
55.5	3.96	12.5

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
71.5	5.11	16.2
239.5	17.11	54.8

Note: Applicable to GD32F101xx and GD32F103xx whose flash capacity does not exceed 128KB.

Table 2-8. f_{ADC}=42MHz Relationship between Sampling period and External input impedance

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
1.5	0.11	0.8
7.5	0.54	6.4
13.5	0.96	11.9
28.5	2.04	25.7
41.5	2.96	37.6
55.5	3.96	50.5
71.5	5.11	65.2
239.5	17.11	219.8

Note: Applicable to GD32F105xx, GD32F107xx, and GD32F101xx and GD32F103xx products whose flash capacity is larger than 128KB.

The integral linear error (ILE) and differential linear error (DLE) of the ADC module depend on the design of the ADC module, and it is difficult to calibrate them. Doing multiple conversions and averaging reduces their impact. Offset and gain errors can simply be compensated using the self-calibration function of the ADC module. Factors affecting ADC accuracy are as follows.

1. Power supply noise, especially high frequency noise linear regulator of switching power supply (SMPS) has better output. It is strongly recommended to connect the filter capacitor at the output end of the rectifier.
2. If switching power supply is used, it is recommended to use a linear voltage regulator for the analog part of the power supply.
3. It is recommended that a capacitor with high frequency characteristics be connected between the power cable and the ground cable, that is, a capacitor of 0.1μF and a capacitor of 1-10 μF should be placed near the power supply end.
4. A separate decoupling capacitor is required for each pair of V_{DD} and V_{SS} pins.
5. V_{DDA} pins must be connected to 2 external decoupling capacitors (10nF ceramic capacitor +1μF tantalum or ceramic capacitor).
6. For 100-pin packages, an external ADC reference input voltage can be connected to V_{REF+} to improve accuracy against low input voltages.
7. Add an external filter to eliminate high-frequency noise.
8. The ground wire is arranged around the analog signal line to produce shielding, which can effectively reduce the crosstalk noise.

2.5.4. DAC Circuit

The digital/analog converter of GD32F10x can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, the DAC output buffer can be used to obtain higher drive capability. The two DACs can work independently or concurrently.

Table 2-9. DAC Related Pin Description

Name	Description	Signal type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
V_{REFP}	DAC positive reference voltage, $2.4V \leq V_{REFP} \leq V_{DDA}$	reference voltage
DAC_OUTx	DACx analog output	Analog output signal

Before enabling the DAC module, the GPIO port (PA4 corresponds to DAC0, PA5 corresponds to DAC1) should be configured in analog mode.

2.5.5. USB Circuit

The GD32F103xx series products contain only USBD modules, while the GD32F105xx and GD32F107xx series are USBFS modules.

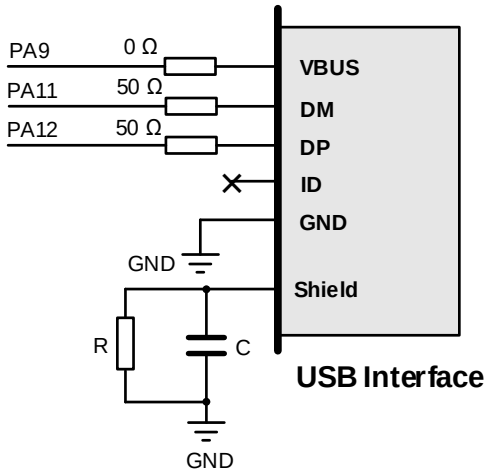
USB protocol requires clock accuracy not less than 500ppm, IRC8M may not be able to achieve such accuracy, so it is recommended to use the USB function when using external crystal or active crystal as the USB module clock source.

The DP line of GD32F103xx series USBD must be externally connected with 1.5K pull-up resistor.

The GD32F105xx and GD32F107xx series USB can be designed as both USB device and USB host.When designed as Device, if PA9 is connected to VBUS, the DP line does not need to be connected with 1.5K pull-up resistor. If PA9 is not connected to VBUS, the DP line must be connected with 1.5K pull-up resistor.

When designing the circuit, in order to improve the ESD performance of USB, it is recommended to design the resistance and capacitance discharge isolation circuit of USB enclosure.

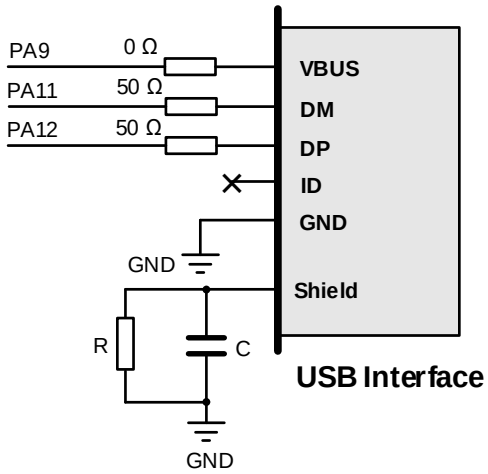
Figure 2-29. Recommend USB-Device Reference Circuit



Recommended：R = 1MΩ，C = 4700 pF.

Note: Only applicable to GD32F103xx.

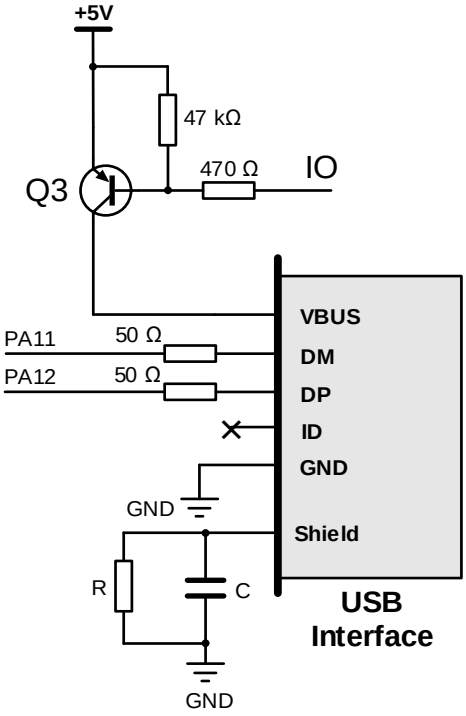
Figure 2-30. Recommend USB-Device Reference Circuit



Recommended：R = 1MΩ，C = 4700pF.

Note: Applicable to GD32F105xx and GD32F107xx products.

Figure 2-31. Recommend USB-Host Reference Circuit



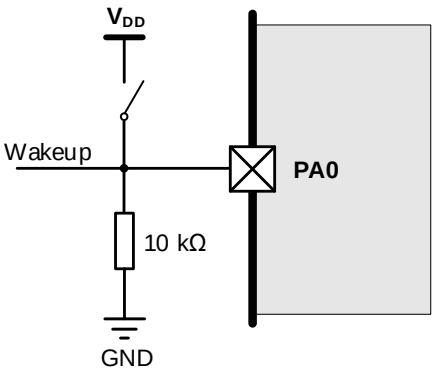
Recommended：R = 1MΩ，C = 4700pF.

Note: Applicable to GD32F105xx, GD32F107xx series products.

2.5.6. Standby mode wake-up circuit

GD32F10x series supports three low-power modes, namely sleep mode, deep sleep mode and Standby mode. The Standby mode has the lowest power consumption and requires the longest wake up time.To wake up from Standby mode, you can wake up through the rising edge of the WKUP pin. In this case, you only need to configure the WUPEN bit in the PMU_CS register.The WKUP wake-up pin reference circuit is designed as follows:

Figure 2-32. Recommend Standby External Wake-up Pin Circuit Design



Note: In the circuit design of this mode, it should be noted that if there is a series resistance between PA0 and VDD, additional power consumption may be increased.

2.6. Download the debug circuit

GD32F10x series cores support JTAG debug interface and SWD interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces.

Note: After reset, the debug related ports are in input PU/PD mode, where:

PA15: JTDI is in pull-up mode.
PA14: JTCK/SWCLK in pull-down mode.
PA13: JTMS/SWDIO in pull-up mode.
PB4: NJTRST is in pull-up mode.
PB3: JTDO is floating mode.

Table 2-10. JTAG Download Debug Interface Assignment

Alternate function	GPIO Port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-33. Recommend USB-Device Reference Circuit

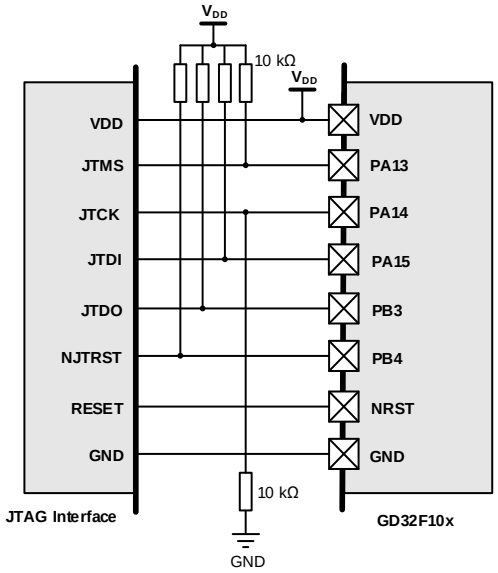
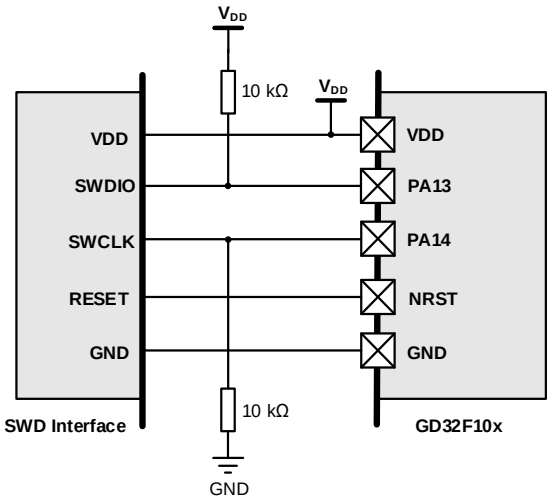


Table 2-11. SWD Download Debug Interface Assignment

Alternate function	GPIO Port
SWDIO	PA13
SWCLK	PA14

Figure 2-34. Recommend SWD Wiring Reference Design

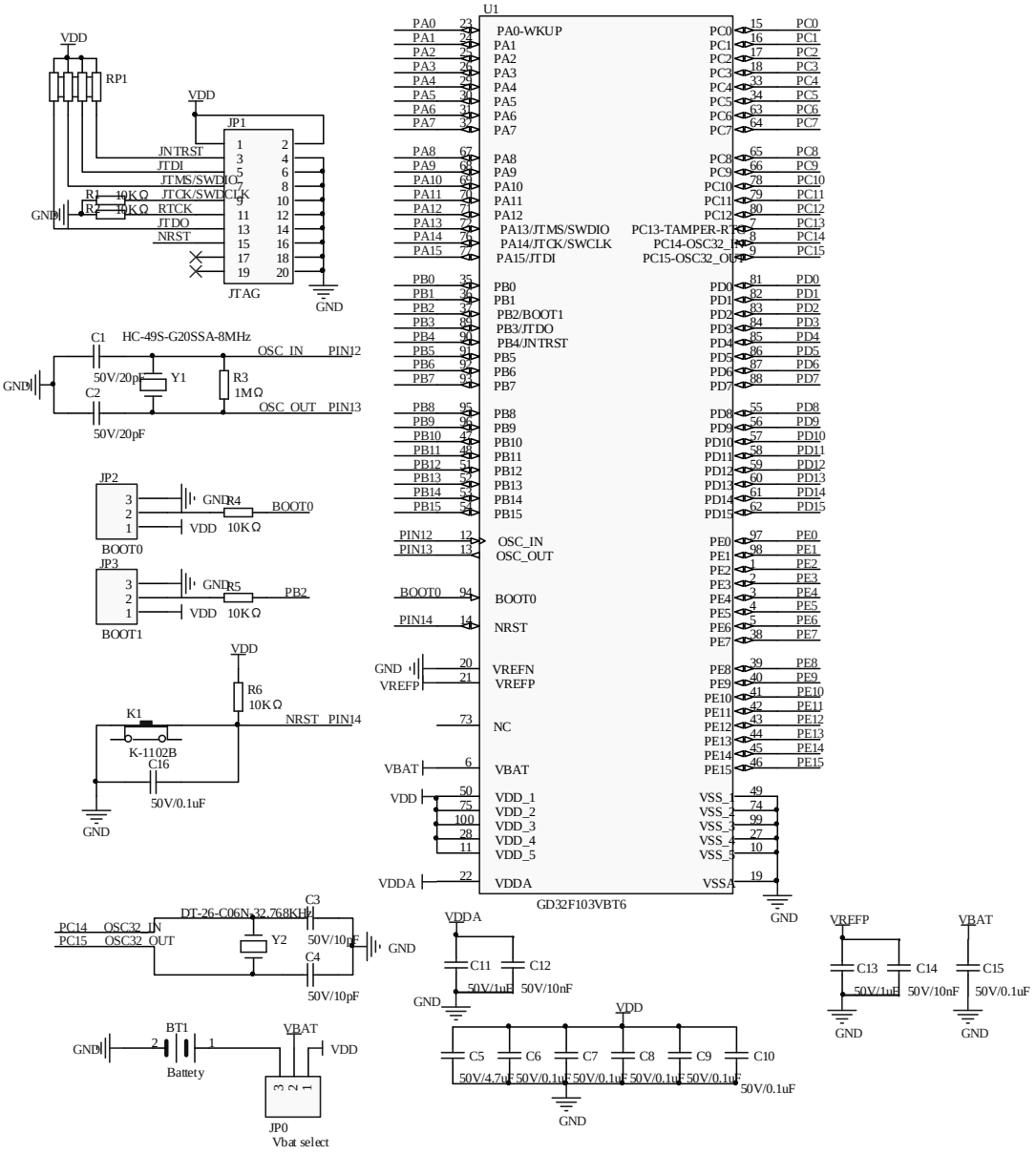


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1kΩ resistor.

2.7. Reference Schematic Design

Figure 2-35. GD32F10x Recommend Reference Schematic Design



3. PCB Layout Design

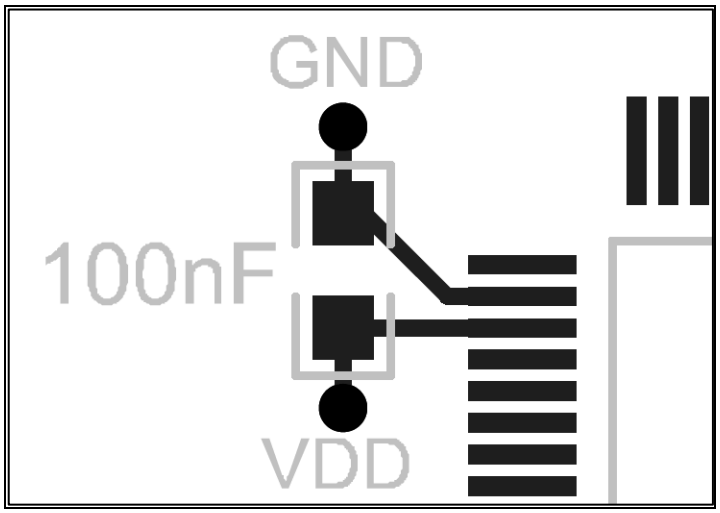
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design scheme with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32F10x series power supply has four power supply pins: V_{DD}, V_{DDA}, V_{REF+} and V_{BAT}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended that you type the Layout in the form of Via near the capacitor PAD.

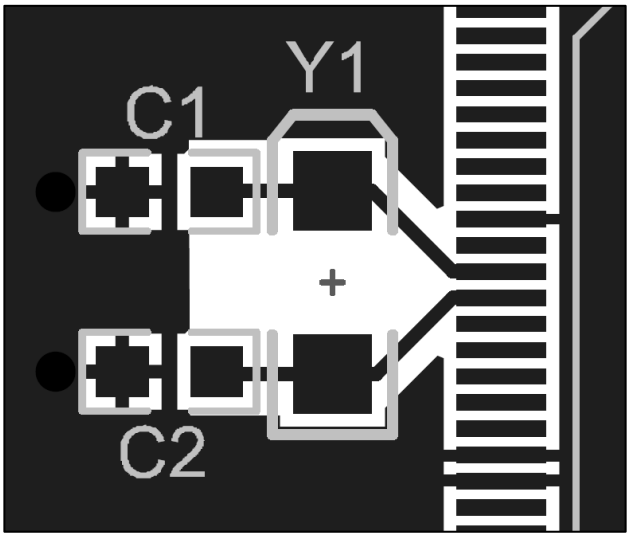
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32F10x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



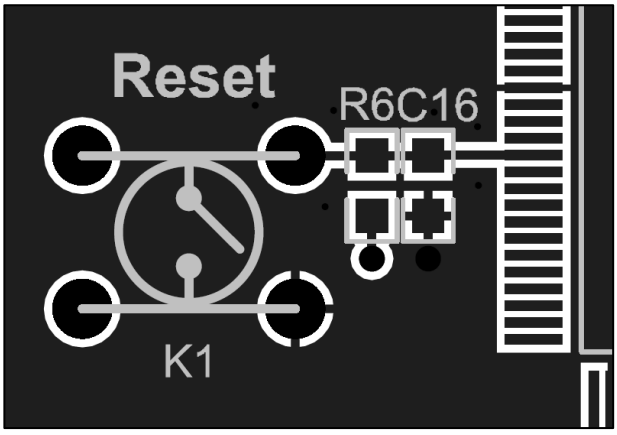
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.
6. The GND of the matching capacitor should be close to the GND of the chip.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong

interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

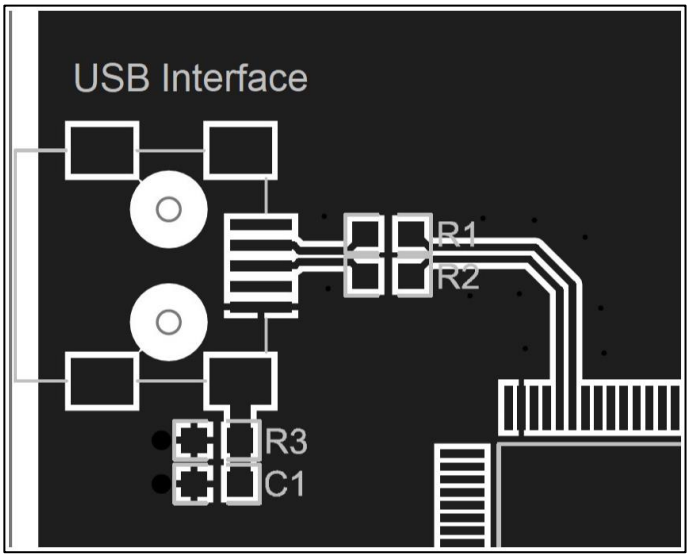
3.4. USB Circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90Ω. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and the traces should be kept as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω. When the USB terminal interface is far away from the MCU, the series resistance value needs to be appropriately increased.

The USB differential trace reference is as follows:

Figure 3-4. Recommend USB Differential Trace Layout Design



Recommendation: R1 = R2 = 50Ω，R3 = 1MΩ，C = 4700pF.

Note:

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

4. Package Description

The GD32F10x series has a total of 5 package types, namely LQFP144, LQFP100, LQFP64, LQFP48, and QFN36.

Table 4-1. Package Description

Ordering code	Package
GD32F101TxU6 GD32F103TxU6	QFN36(6x6, 0.5 pitch)
GD32F101CxT6 GD32F103CxT6	LQFP48(7x7, 0.5 pitch)
GD32F10xRxT6	LQFP64(10x10, 0.5 pitch)
GD32F10xVxT6	LQFP100(14x14, 0.5 pitch)
GD32F10xZxT6	LQFP144(20x20, 0.5 pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct.25, 2022
1.1	Update section 2.1.3 to provide all packaging power supply design drawings, explaining the connection of relevant pins within the chip.	Jun.21, 2023
1.2	Update section 2.1.3, section 2.1.3, Udate NRST related content.	Apr.28, 2024
1.3	Refine the content related to power supply detection and reset, and update Section 2.2, 2.3.	Dec.15, 2024

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.